CMP process innovations, growing needs and challenges imposed by new architectures, new materials and dimensional scaling for logic and advanced interconnects

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Imec is shaping the semiconductor roadmap (today even beyond 1nm), building on different scaling approaches with continued dimensional scaling, device and material innovations and novel chip interconnect architectures. We are establishing a stable, functional baseline for nanosheets, targeting the 2nm node (N2).
We will present a view on program roadmaps and scaling landscapes, diving into the required CMP R&D, as part of our technology development for advanced logic and advanced interconnects (down to N2).

Scaling logic and memory circuits goes hand-in-hand with an improvement of the efficiency of compute. Only scaling the transistors along the logic roadmap is not enough anymore to keep on boosting power and performance. Today we enter the era of interconnects, meaning that we continue scaling logic and memory, but we also built up chips by enabling many more and new type of interconnects with new architectures.
Furthermore the continuous scaling of the device density in both logic and memory circuits entails the dimensional scaling (shrinking) of the interconnect line dimensions.

Today, the characteristic dimensions of BEOL interconnects in state-of-the-art microelectronic chips approach 10 nm and will reach even smaller dimensions in the near future. Extreme Ultraviolet (EUV) lithography is used as a cutting-edge technique to achieve high resolution patterning and to enable connectivity with smaller pitches. The nano interconnect scaling landscape shows boosters like semi damascene approaches with direct metal etch as well as the introduction of alternative metals (replacing Cu to eg Ru) to enable an improved resistance and interconnect reliability. Metal CMP or dielectric gapfill CMP steps are needed in different scaling approaches and boosters, leading to more stringent criteria and challenges for the CMP engineer.

Also for 3D interconnect technology the critical pitch is being reduced, enabling an increased device density and performance. In recent years, new technologies like die-to-wafer (D2W) and wafer-to-wafer (W2W) hybrid bonding have become essential in the development of electronic devices. The continuous scaling to finer pitches for these technologies requires continuous CMP R&D and process adaptation to meet the increasingly more stringent post-CMP nano topography requirements for optimal bonding efficiency.

A glance at the world of heterogeneous integration and the key building blocks - the interconnects, their distance and critical pitches - will make it clear that we have different interconnects and scaling everywhere in the nanosheet era: small pitch connections i(close to 20nm) in backend of line, connections to the backside (improved backside power delivery network, nTSV), scaled (200 nm-pitch) WTW and (2µm-pitch) D2W bond pads and high-density microbumps. We also see emerging Interposer substrates, enabling faster and denser interconnects, where the interposers are being made of Si or made of photo-patternable polymer with fine-pitch redistribution layers.

For the different interconnect technologies, application and material driven CMP solutions are needed and consist of selecting optimal combinations of tool features, process conditions and consumables, considering also the impact of dimensional scaling.
Our CMP R&D for advanced interconnects includes CMP of different gapfill dielectrics (including also polymer) and metals (including materials beyond W and Cu), with stringent and application driven requirements for removal amount (eg from nm dielectric removal in logic to microns in 3Di), planarisation efficiency and stopping capability.
In specific cases we need nanometer topography and/or Angstrom roughness control at CMP, often being used as a surface preparation technique eg pre bonding. In other cases we need to be able to handle several microns thick gapfill materials (eg dielectrics and Cu in 3Di). The variety of materials also imposes the complexity of needing compatibility with these materials and avoiding a high level of post CMP defects like scratches or eg metal corrosion. All this comes on top of design related aspects, where in several cases design modifications are required to lead to a more CMP friendly design with an improved CMP performance.