Advanced Ceria Slurries for SiO_2 CMP: Polishing Mechanism of Nanoceria and Emerging Applications

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Owing to the strong chemical affinity between ceria abrasives and SiO_2 surfaces, ceria-based slurries have been widely adopted for SiO_2 chemical mechanical planarization (CMP), particularly in shallow trench isolation (STI) and interlayer dielectric (ILD) applications. Resonac has developed a broad portfolio of ceria abrasives, ranging from conventional large-particle calcined ceria to single-nanometer-scale ceria abrasives, referred to as “Nanoceria,” and these materials have supported memory and logic device manufacturing for several decades.

As device dimensions continue to shrink and defectivity requirements become increasingly stringent, there is a growing need for slurry technologies that simultaneously provide sufficient SiO_2 removal rate, high planarization performance, and low scratch generation. Nanoceria has been developed to address these requirements by combining the intrinsic chemical reactivity of ceria with finely controlled abrasive size and dispersion stability. In contrast, calcined ceria remains attractive for applications requiring high removal rate and robust process windows, although further optimization is needed to meet emerging defectivity targets.

This presentation will discuss the unique reactivity of Nanoceria slurries and the proposed polishing mechanism, supported by analytical characterization of abrasive–surface interactions and polishing behavior. In addition, potential application areas for ceria slurry adoption in advanced logic, memory, and packaging processes will be introduced, together with the remaining technical challenges for extending ceria CMP to next-generation semiconductor manufacturing.

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